

Applicant(s): Antonius Henricus Maria Raaijmakers et al.
Serial No.: 09/745,914
For: ELECTRO-OPTICAL DEVICE HAVING AN ITO LAYER, A SiN LAYER AND AN
INTERMEDIATE SILICON OXIDE LAYER
Filed: December 22, 2000
Examiner: Chung, David Y.
Group Art Unit: 2871

Attorney Docket No.: PHN 17,819

REMARKS/ARGUMENTS

Claims 1, 2 and 4 through 6 are pending in the present application. Claims 1, 4 and 6 have been amended.

The Action (1) rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Bird et al. reference (*Large-area image sensing using amorphous silicon nip diodes*, N.C. Bird, C.J. Curling, C. van Berke, Sensors and Actuators A 46-47 (1995) 444-448.) (hereafter “the Bird reference”) in view of Japanese Patent No. JP 01-245226 to Tanaka (hereafter “the Tanaka reference”); and (2) rejected claims 4 through 6 under 35 U.S.C. 103(a) as being unpatentable over the Bird reference in view of Japanese Patent No. JP 01-245226 to Tanaka (hereafter “the Tanaka reference”) and in further view of U.S. Patent No. 5,135,581 to Tran et al. (hereafter “the ‘581 patent”).

Regarding item (1) identified above, it is respectfully submitted that the cited reference combination fails as the Tanaka reference specifically teaches away from that which is suggested and/or disclosed in the Bird reference as well as the invention of present claim 1. That is to say, the Tanaka reference specifically teaches that “the silicon oxide layer 7 is formed at the same pattern as the pattern of the ITO layer 6 on the ITO layer 6”. Whereas the Bird reference contrastingly suggests that only a portion of an indium tin oxide (ITO), located on top of the diode stacks, is appropriate for the deposition of a silicon oxide layer (i.e., the top of the photodiode PD is such that light can enter through the transparent ITO layer/electrode). Likewise, present claim 1 has a portion of the ITO layer (i.e., the photosensitive element) not intended for having a silicon oxide layer deposited thereon.

Thus, it is respectfully submitted that the Tanaka reference, which specifically requires that a silicon oxide layer have the same pattern as the ITO layer on which it is deposited, teaches away from that which is provided by the Bird reference. Hence, there is not motivation to combine the cited references. Moreover, the Tanaka reference also teaches away from the

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invention of claim 1, which has “at least one photosensitive element and at least one switching element” with at least one layer of amorphous silicon on which an ITO (indium tin oxide) layer is provided...[and only]...said at least one switching element is completely shielded during manufacture”. Hence, the silicon oxide layer does not have the same pattern as the ITO layer. Accordingly, as the Tanaka reference teaches away from the claimed invention [*In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997)], reconsideration and withdrawal of the stated rejection under 35 U.S.C. 103(a) of claim 1, and allowance thereof, are respectfully requested.

With regard to claim 2, which depends directly from claim 1, it is respectfully submitted that such claim is patentable at least for the reasons discussed above with respect to claim 1. Accordingly, reconsideration and withdrawal of the rejection, and allowance of claim 2, are respectfully requested.

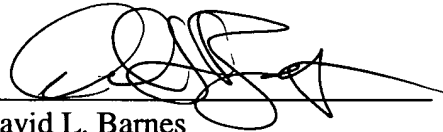
Regarding item (2) identified above, it is respectfully submitted that present claim 4 is patentable over the cited reference combination at least for the reasons discussed above with respect to claim 1. That is, [1] there is no motivation to combine the references as the Tanaka reference, which requires that a silicon oxide layer have the same pattern as the ITO layer on which it is deposited, teaches away from that which is provided by the Bird reference; and moreover [2] the Tanaka reference specifically teaches away from the invention of claim 4, which has “at least one photosensitive element and at least one switching element” with at least one layer of amorphous silicon” and includes a step of “depositing a doped ITO layer on said at least one layer of amorphous silicon” and further provides that only “said at least one switching element is completely shielded during manufacture”. Thus, the silicon oxide layer does not have the same pattern as the ITO layer. Accordingly, reconsideration and withdrawal of the stated rejection of claims 4-6, claims 5 and 6 being directly or indirectly dependant on claim 4, and allowance of such claims, are respectfully requested.

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In sum, it is respectfully submitted that the cited reference combination fails and moreover that the present pending claims are patentable over such reference combination. Thus, this application is in condition for allowance. Accordingly, reconsideration and withdrawal of all rejections of the claims are respectfully requested.

Respectfully submitted,



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